AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A ~~cell element field for~~ data processing arrangement, comprising: ~~having~~

a cell element field including:

a plurality of function cell arrangements [[means]] configured to ~~for executing~~ execute at least one of algebraic and ~~and/or~~ logic functions; [[and]]

a plurality of memory cell arrangements [[means]] configured to at least one of receive, store, and ~~and/or~~ output information; and

for at least one of the plurality of function cell arrangements and at least one of the plurality of memory cell arrangements, a connection via which the at least one function cell is connectable with the at least one memory cell to form a ~~,wherein~~ function cell-memory cell combination ~~combinations are formed in which a control connection leads from the function cell means to the memory cell means~~ that is configured to function as a sequencer structure that provides control commands from the at least one function cell arrangement to the at least one memory cell arrangement via the connection.

2. (Currently Amended) The ~~cell element field~~ data processing arrangement as recited in ~~the preceding~~ claim 1, wherein:

at least one of the ~~a processor, coprocessor and/or microcontroller forms a~~ plurality of function cell arrangements ~~units~~ and the plurality of ~~such as function cells and/or~~ memory cell arrangements are at least one of reconfigurable and preselectable in at least one of their ~~cells whose~~ function and their ~~and/or~~ interconnection ~~is/are reconfigurable and/or preselectable~~; and

the cell element field forms at least one of a processor, a coprocessor, and a microcontroller.

3. (Currently Amended) The ~~cell element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 1, wherein the function cell arrangements [[cells]] are formed as arithmetic logic units.

4. (Currently Amended) The ~~cell-element field~~ data processing arrangement as recited in ~~the preceding~~ claim 3, wherein the arithmetic logic units are formed as extended ALUs.

5. (Currently Amended) The ~~cell-element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 1, wherein the memory cell arrangements [[cells]] are designed as at least one of volatile and ~~and/or~~ nonvolatile data memories.

6. (Currently Amended) The ~~cell-element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 1, wherein the memory cell arrangements [[cells]] are designed for at least one of storage of data to be processed and ~~and/or~~ program steps to be executed.

7. (Currently Amended) The ~~cell-element field for~~ data processing arrangement as recited in claim 1, wherein the memory cell arrangements [[cells]] are designed such that, in response to at least one of the control commands, the at least one memory cell arrangement sends ~~for sending~~ stored information at least one of directly and ~~and/or~~ indirectly to a bus leading to the at least one function cell arrangement ~~in response to triggering by the function cell which controls them~~.

8. (Currently Amended) The ~~cell-element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 7, wherein the stored information is sent to the at least one function cell arrangement via ~~registers, in particular~~ a backward register which is situated in an [[the]] information path between the at least one memory cell arrangement and the at least one function cell arrangement ~~, are assigned to at least one memory cell and/or function cell~~.

9. (Currently Amended) The ~~cell-element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 1, wherein the at least one memory cell arrangement is configured ~~situated~~ to receive information from at least one of the at least one function cell arrangement ~~which controls it~~, an input-output cell, and ~~and/or~~ a cell having an arithmetic logic unit that does not provide control commands to the at least one memory cell arrangement ~~control it~~.

10. (Currently Amended) The ~~cell element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 1, wherein at least one input-output arrangement [[means]] is assigned to the function cell-memory cell combination for at least one of sending information to and receiving information from at least one of an external unit, ~~and/or~~ another function cell arrangement, another function cell-memory cell combination, and another ~~and/or~~ memory cell arrangement ~~and/or for receiving information from it~~.

11. (Currently Amended) The ~~cell element field~~ data processing arrangement as recited in ~~the preceding~~ claim 10, wherein the at least one input-output arrangement [[means]] is [[are]] also designed to receive control commands from the at least one function cell arrangement.

12. (Currently Amended) The ~~cell element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 10, wherein at least one of the at least one function cell arrangement ~~controller is designed~~ configured to transmit and at least one of the at least one memory cell arrangement and the at least one input-output arrangement is configured to decode at least some ~~, preferably all of the following commands, and/or the memory cell and/or input-output cell is designed to decode the following commands:~~ of a DATA WRITE/READ command, an ADDRESS POINTER WRITE/READ command, a PROGRAM POINTER WRITE/READ command, a PROGRAM POINTER INCREMENT command, and a STACK POINTER WRITE/READ command, ~~said commands in particular for internal and/or external access,~~ a PUSH command, a POP command, an OPCODE command, and a FETCH command, at least some of said commands being for at least one of internal and external access.

13. (Currently Amended) The ~~cell element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 1, wherein the at least one function cell arrangement is configured as [[the]] a sole master that is able to access at least one of the ~~control~~ connection and a ~~and/or the~~ bus segment functioning as the ~~control~~ connection.

14. (Currently Amended) The ~~cell element field for~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 10, wherein the at least one function cell arrangement is situated adjacent to at least one of: (a) the at least one memory cell arrangement; and (b) ~~and/or~~ the at least one input-output arrangement [[cell]].

15. (Currently Amended) The ~~cell element field~~ data processing arrangement as recited in ~~one of the preceding claims~~ claim 10, wherein:

the cell element field is a multidimensional cell element matrix; ~~elements are arranged multidimensionally, in particular in a matrix,~~

the at least one function cell arrangement is situated adjacent the at least one memory cell arrangement on a same row of the matrix;

the input-output arrangement is situated on the same row;

at least one of the at least one function cell arrangement, ~~and/or~~ the ~~adjacent~~ at least one memory cell arrangement, and ~~and/or~~ the at least one input-output arrangement is ~~cell being~~ able to receive data from an upper row and output data into a lower row [[,]] via buses ~~being provided in one row and the function cell and at least one memory cell and/or input-output cell being situated in one and the same row~~.

16. (Currently Amended) A method for operating a data processing arrangement including ~~cell element field, in particular~~ a multidimensional cell element field, the cell element field including a plurality of ~~having~~ function cell arrangements configured to execute ~~cells for execution~~ at least one of algebraic and ~~and/or~~ logic functions and a plurality of ~~information providing cells, in particular~~ memory cell arrangements ~~cells and/or input-output cells for receiving and/or outputting and/or storing~~ configured to at least one of receive, store, and output information, the method comprising:

~~wherein~~ operating at least one of the plurality of function cell arrangements of the cell element field as a sequencer to output ~~cells outputs~~ control commands to at least one of the plurality of memory ~~information providing~~ cell arrangements of the cell element field ~~, [the information] is processed there in response to the control command information for the function cell, and the function cell is designed to perform further data processing in response to the information provided from the information providing cell in order to process data in the manner of a sequencer~~.

17. (Currently Amended) The method as recited in ~~one of the preceding claims~~ claim 16, further comprising: ~~wherein~~

the at least one function cell arrangement outputting during operation of at least one cell element of the cell element field ~~is designed [to output]~~ at least some of ~~the control commands~~ an OPCODE FETCH command, a DATA WRITE INTERNAL, a DATA WRITE EXTERNAL command, a DATA READ INTERNAL command, a DATA READ EXTERNAL command, an ADDRESS POINTER WRITE INTERNAL command, an ADDRESS POINTER WRITE EXTERNAL command, an ADDRESS POINTER READ INTERNAL command, an ADDRESS POINTER READ EXTERNAL command, a PROGRAM POINTER WRITE INTERNAL command, a PROGRAM POINTER WRITE EXTERNAL command, a PROGRAM POINTER READ INTERNAL command, a PROGRAM POINTER READ EXTERNAL command, a STACK POINTER WRITE INTERNAL command, a STACK POINTER WRITE EXTERNAL command, a STACK POINTER READ INTERNAL command, a STACK POINTER READ EXTERNAL command, a PUSH command, a POP command, and a PROGRAM POINTER INCREMENT command ~~and in the course of cell element operation to output at least some, in particular all, of the control commands indicated above as necessary~~.

18. (New) The data processing arrangement as recited in claim 1, wherein the at least one memory cell arrangement includes a data output separate from the connection.

19. (New) The data processing arrangement as recited in claim 1, wherein the at least one memory cell arrangement includes at least two pointers configured to address at least two of a stack, a heap, and a program.

20. (New) The method as recited in claim 16, wherein the at least one memory cell arrangement includes a data output separate from a connection via which the control commands are output from the at least one function cell to the at least one memory cell.

21. (New) The method as recited in claim 16, wherein the at least one memory cell arrangement includes at least two pointers configured to address at least two of a stack, a heap, and a program.